CLAIMS

What is claimed is:

1. A vertical surface mount semiconductor device, comprising:

a semiconductor device;

a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof; and

conductive bumps disposed adjacent selected bond pads, each of said conductive bumps configured to form a conductive joint between one of said selected bond pads and a corresponding terminal of a substrate upon positioning said semiconductor device substantially vertically relative to said substrate.

2. The vertical surface mount semiconductor device of claim 1, wherein a conductive bump is disposed adjacent each of said plurality of bond pads.

3. The vertical surface mount semiconductor device of claim 1, further comprising a support layer.

4. The vertical surface mount semiconductor device of claim 3, wherein said support layer is disposed on another surface of said semiconductor device.

5. The vertical surface mount semiconductor device of claim 1, further comprising a support footing formed adjacent said edge.

6. The vertical surface mount semiconductor device of claim 5, wherein said support footing is disposed on another surface of said semiconductor device.

7. The vertical surface mount semiconductor device of claim 5, wherein said support footing is disposed on said surface of said semiconductor device.

8. The vertical surface mount semiconductor device of claim 1, further comprising a laminate which connectively bonds said semiconductor device to an adjacent semiconductor device.

9. A vertical surface mount semiconductor device, comprising:

a semiconductor device;

a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof, selected bond pads of said plurality of bond pads having conductive bumps adjacent thereto, said conductive bumps configured to form a joints between said selected bond pads and corresponding terminals of a carrier substrate upon substantially perpendicular orientation of said semiconductor device on said carrier substrate; and

a support member, at least a portion of which is disposed proximate said edge of said semiconductor device.

10. The vertical surface mount semiconductor device of claim 9, wherein said support member is selected from the group consisting of support footings and support layers.

11. The vertical surface mount semiconductor device of claim 9, wherein said support member is disposed on another surface of said semiconductor device.

12. The vertical surface mount semiconductor device of claim 9, wherein a conductive bump is positioned adjacent each of said plurality of bond pads.

13. A chip-on-board assembly, comprising:

a substrate with a plurality of terminals;

a semiconductor device configured to be positioned substantially perpendicularly relative to said substrate, said semiconductor device having a plurality of bond pads on a

surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface; and

electrically conductive joints configured to be disposed and to establish communication between selected bond pads and corresponding terminals.

14. The chip-on-board assembly of claim 13, wherein each of said plurality of bond pads has an electrically conductive joint disposed adjacent thereto.

15. The chip-on-board assembly of claim 13, further comprising a support member in contact with at least one of said semiconductor device and said carrier substrate.

16. The chip-on-board assembly of claim 15, wherein said support member is selected from the group consisting of support footings and support layers.

17. The chip-on-board assembly of claim 15, wherein said support member is disposed proximate said edge of said semiconductor device.

18. The chip-on-board assembly of claim 13, wherein said semiconductor device is laminated to an adjacent semiconductor device.

19. A computer including a vertically mountable semiconductor device, the semiconductor device comprising:

a semiconductor die with a plurality of circuit traces;

a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof, each of said plurality of bond pads communicating with one of said plurality of circuit traces; and

conductive bumps in communication with selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a

corresponding terminal of a substrate when said semiconductor device is positioned substantially perpendicularly relative to said substrate.

20. The computer of claim 19, wherein each of said plurality of bond pads has a conductive bump in communication therewith.

21. The computer of claim 19, wherein said semiconductor device further comprises a support member.

22. The computer of claim 21, wherein said support member is selected from the group consisting of support footings and support layers.

23. The computer of claim 21, wherein said support member is disposed proximate said edge.

24. The computer of claim 19, wherein said semiconductor device is laminated to an adjacent semiconductor device.